CLAIMS

What is claimed is:

I claim:

manufacturing a processor having a flexible architecture to service multiple processor platforms as well as different application platforms.

- 2. The method of claim 1, further comprising:

 manufacturing the processor to communicate with a device through a point to point bus.
- 3. The method of claim 1, further comprising:

 manufacturing an arbiter to alter one or more signal pathways that a signal may travel

 within the processor, the arbiter can alter the signal pathways without physically changing the

 flexible architecture inside the processor.
- 4. An apparatus, comprising
 an arbiter linked to a first processor having a flexible architecture;
 a point to point bus; and
 a device, the first processor connected to the device through the point to point bus.
- 5. The apparatus of claim 4, wherein the arbiter is internal to the first processor.

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- 6. The apparatus of claim 4, wherein the arbiter is external to the first processor.
- 7. The apparatus of claim 4, wherein the arbiter comprises a component to change a number of ports linked between the first processor and the device without changing the flexible architecture within the processor.
- 8. The apparatus of claim 4, wherein the device is selected from the group consisting of an input-output component, a bridge, a chipset, a memory, or a second processor.
- 9. The apparatus of claim 4, wherein the processor comprises:

a protocol layer;

an information transfer layer to electronically transfer information on a physical medium between the protocol layer and the device; and

a buffer layer to buffer an electronic transfer of information between the protocol layer and the information transfer layer.

10. The apparatus of claim 4, wherein the arbiter comprises a first component and a second component, the first component to determine a bandwidth between the device and the processor, the second component to provide a control signal to one or more signal pathway switching devices, the control signal to be based upon the bandwidth determination of the first component.

11. A method; comprising:

communicating between a processor and a device through a point to point bus;
using a signal pathway internal to the processor during the communications between the
processor and the device; and

changing the signal pathway within the processor to optimize a connection for an application.

- 12. The method of claim 11, wherein to optimize a connection comprises altering the bandwidth between a first processor and a device exterior to the first processor.
- 13. The method of claim 11, wherein to optimize a connection comprises altering a number of processors connected to the device.
- 14. The method of claim 11, wherein the application is selected from a group consisting of a work station application, a server application, a two processor platform, a four processor platform, or an eight processor platform.
- 15. The method of claim 11, wherein the changing of the signal pathway consists of changing a setting in a configuration register to direct an arbiter to send a control signal to one or more signal pathway switching devices located in the processor.
